Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) A multiplication apparatus for multiplying a multi-bit multiplier and a multi-bit multiplicand, comprising:

a Booth encoder for encoding said multiplier in accordance with a Booth algorithm for generating a plurality of select control signals;

Booth selection circuitry for generating a plurality of partial products in accordance with said plurality of select control signals received from said Booth encoder and said multi-bit multiplicand;

intermediate product generating circuitry for adding said plurality of partial products generated by said Booth selection circuitry in a tree-like form and sequentially reducing a number of said partial products to generate final intermediate multiplication values, said intermediate product generating circuitry having a divided array arrangement of being divided into two divided arrays at a prescribed bit position of said multi-bit multiplier, said two divided arrays concurrently performing addition operation and independently generating said final intermediate multiplication values, respectively, of each other and each of the divided arrays including a plurality of stages of addition circuits arranged in a Wallace tree configuration to perform addition in said tree-like form and a Booth selection circuit of said Booth selection circuitry; and

a final addition circuit for adding said final intermediate multiplication values from said intermediate product generating circuitry for generating a multiplication value of said multi-bit

multiplier and said multi-bit multiplicand, the final intermediate multiplication value of each divided array being transmitted to said final addition circuit without passing over another divided array.

2. (Original) The multiplication apparatus according to claim 1, wherein the divided arrays are arranged in a direction orthogonal to a direction in which said plurality of select control signals are transmitted,

said final addition circuit is arranged between said divided arrays, and

a tree-like array of the addition circuits in each of said divided arrays performs the addition in said tree-like form in a direction toward said final addition circuit.

3. (Original) The multiplication apparatus according to claim 2, wherein the addition circuits arranged in said plurality of stages include different addition circuits with different bit widths,

the addition circuits in said plurality of stages are arranged in corresponding divided arrays with their one-ends aligned and their other ends positioned according to respective bit widths, and

said Booth encoder is arranged on a side of the other ends.

4. (Original) The multiplication apparatus according to claim 3, wherein said Booth encoder is arranged being divided to sandwich said final addition circuit.

5. (Original) The multiplication apparatus according to claim 1, further comprising a multiplicand generating circuit receiving said multi-bit multiplicand for application to said Booth selection circuitry, wherein said multiplicand generating circuit is arranged between said divided arrays.

6. (Withdrawn) The multiplication apparatus according to claim 1, wherein said divided arrays are arranged in a direction in which said plurality of select control signals are transmitted, and each of said divided arrays includes the addition circuits arranged in the plurality of stages for adding the partial products in a tree-like form in a same direction.

7. (Withdrawn) The multiplication apparatus according to claim 6, wherein said Booth encoder is divided to be arranged facing to each of said divided arrays.

8. (Withdrawn) The multiplication apparatus according to claim 7, wherein each of said divided arrays includes the addition circuits in the plurality of stages having different bit widths,

said addition circuits in said plurality of stages have their one-ends aligned, and

the Booth encoder is arranged on a side of other ends of said addition circuits in said plurality of stages.

9. (Withdrawn) The multiplication apparatus according to claim 8, wherein said Booth encoder is arranged on opposite sides with respect to said divided arrays.

10. (Withdrawn) The multiplication apparatus according to claim 8, wherein said Booth encoder is arranged between said divided arrays.

11. (Withdrawn) The multiplication apparatus according to claim 6, further including a multiplicand data generating circuit for applying said multi-bit multiplicand to said Booth selection circuitry, wherein

said multiplicand data generating circuit is arranged commonly to said divided arrays and facing to one of said divided arrays.

12. (Withdrawn) The multiplication apparatus according to claim 6, further including a multiplicand data generating circuit for applying said multi-bit multiplicand to said Booth selection circuitry, wherein

said multiplicand data generating circuit is arranged in a region between said divided arrays.

13. (Withdrawn) The multiplication apparatus according to claim 9, further including a multiplicand data generating circuit for applying said multi-bit multiplicand to said Booth selection circuitry, wherein

said multiplicand data generating circuit is arranged between said divided arrays.

14. (Withdrawn) The multiplication apparatus according to claim 10, further including a multiplicand data generating circuit for applying said multi-bit multiplicand to said Booth selection circuitry, wherein

said multiplicand data generating circuit is arranged, adjacent to said Booth encoder, between said divided arrays.

15. (Withdrawn) The multiplication apparatus according to claim 12, wherein said multiplicand generating circuit is so formed into a divided structure as to have a height according to a height of said divided arrays in a direction orthogonal to a direction in which the select control signals are transmitted.

16. (Withdrawn) The multiplication apparatus according to claim 6, wherein said final addition circuit is arranged commonly to said divided arrays for adding the final intermediate multiplication values from said divided arrays and producing a final product as said multiplication value.